In the Specification

Please amend paragraph [0023] as following.

[0023] Figure 4 shows the schematic drawing of the DDR termination array of the present invention, which comprises a plurality of resistors 161, a plurality of signal terminals 163, a plurality of switches 162 and an enable pin EN. Each of the resistors 161 has a first terminal 161a and a second terminal 161b. The first terminals 161a respectively connect with the voltage source V_{TT}, so that the resistors are functioned as termination resistors. The second terminals 161b connect with relative signal terminals 163 via switches 162. Each switch in the embodiment has a first terminal, a second terminal and a control terminal. All the first terminals connect with their corresponding signal terminals, respectively. The control terminals are coupled to the enable pin EN that is used to determine whether all the switches are conducted or not. When the enable pin delivers an enable state, the switches are conducted and signals can be output from the signal terminals. When the enable pin EN delivers a disable state, the switches are open to prevent signals from being output from associated signal terminals. The switches can be established by using transmission gates.